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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,669	03/06/2002	Jeremy D. Dunworth	010481	3826

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EXAMINER	
NGUYEN, THUAN T	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,669	DUNWORTH ET AL.	
	Examiner	Art Unit	
	THUAN T. NGUYEN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,17-22 and 34-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,17-22 and 34-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-8, 17-22, and 34-45 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

3. Claims 1-8, 17-22, and 34-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (US Patent 6,137,372) in view of Binder (US Patent 5,892,408).

Regarding claim 1, Welland discloses "a method of calibrating an oscillator comprising: generating a first signal indicative of an initial frequency of the oscillator for an input parameter; generating a second signal indicative of a reference frequency, wherein generating the first and second signals comprises scaling the initial frequency of the oscillator and the reference frequency at approximately the same time so that the generated signals are substantially in phase; and adjusting the initial frequency of the oscillator based on a comparison of the first and second signals", i.e., Welland in Figure 5 describes an exact procedure in calibrating an oscillator within a frequency synthesizer 500 as Vint 504 generates an initial frequency at the VCO 400 and f ref 106 is generated as a reference frequency, and the two signals are compared based on phase detector 206 and the initial frequency of the oscillator is adjusting based on the comparison of

both signals at the same time (col. 8/line 58 to col. 10/line 11 as either analog control loop and digital control loops are active at the same time, and as in col. 3/lines 30-64 for the objective of Welland).

Welland does not clearly show the first and second signals are generating substantially in phase for calibration the oscillator; however, Binder clearly show with a temperature sensor, a frequency reference and a logic timing and control unit, the first and second signals are generating substantially in phase for calibration the oscillator (Figs. 4-5, and col. 7/line 57 to col. 8/line 25). Therefore, it would have been obvious to one of ordinary skill in the art to modify Welland's with Binder's teaching technique as noted in order to provide the first and second signals are generating substantially in phase for calibration the oscillator as desired.

As for claim 2, in view of claim 1, Welland discloses "wherein the oscillator comprises a voltage controlled oscillator and the input parameter comprises a calibration voltage input, and wherein generating the first signal comprises applying the calibration voltage input to the voltage controlled oscillator to generate the initial frequency of the oscillator and scaling the initial frequency of the oscillator" (Fig. 5 for VCO 400, Vint 504 for initial voltage input in generating initial frequency of the oscillator, and Vc or voltage control input, and the discrete control 502 monitors and controls the f out 102 in adjusting or calibrating the initial control voltage at node 510 for scaling the initial frequency of the oscillator again, see col. 9/lines 12-54).

As for claim 3, in view of claim 2, Welland shows "further comprising generating the calibration voltage input based on temperature" (col. 7/line 65 to col. 8/line 25 as due to temperature variations, the continuously variable capacitance 406 is used for any post calibration frequency drift, col. 8/lines 12-25 & col. 10/lines 2-16).

As for claim 4, in view of claim 1, Welland discloses further "comprising enabling a phase locked loop after adjusting the initial frequency and testing a voltage control input to the oscillator from the phase locked loop to determine whether calibration should be performed again" (Fig. 2 for a PLL, and PLL is used in Welland, col. 9/lines 11-33 & col. 3/lines 35-54 as PLL is needed for the determination of whether calibration should be performed again).

As for claim 5, in view of claim 1, Welland discloses "wherein generating the second signal comprises receiving the reference frequency from a temperature compensated crystal oscillator and scaling the reference frequency" (Fig. 1/item 105 for a crystal oscillator in generating a reference frequency, col. 5/lines 40-58).

As for claim 6, in view of claim 1, Wellnad discloses "wherein scaling the initial frequency of the oscillator and scaling the reference frequency at approximately the same time comprises initializing divider circuits for the initial frequency of the oscillator and the reference frequency at approximately the same time", i.e., a frequency divider circuit is used for scaling and initializing the divider circuits for the initial frequency of the oscillator (Fig. 5 for frequency synthesizer with frequency divider circuits with divide by R 204 and divide by N 214, with technique as disclosed earlier in claim 1 above for generating the initial frequency of the oscillator and both frequency signals at approximately the same time).

As for claim 7, in view of claim 1, Welland discloses "wherein the oscillator comprises a voltage controlled oscillator including a number of switched capacitors, and wherein adjusting the initial frequency of the oscillator based on a comparison of the first and second signals comprises activating a subset of the switched capacitors based on the comparison of the first and

second signals" (Fig. 7 and col. 13/line 35 to col. 14/line 42 for a capacitor switch circuits addressed).

As for claim 8, in view of claim 1, Welland further discloses "comprising enabling a phase lock loop following calibration of the oscillator, and adjusting an initial gain of a charge pump of the phase lock loop based on a calibration setting of the oscillator" (Fig. 5, and col. 8/line 58 to col. 9/line 5, again, the calibration procedure includes a PLL 500, an initial gain of a charge pump 208 of the PLL can be adjusted based on the calibration setting or control of the discrete control block 502 as if a big error is detected, the control block 502 adjusts the calibration by switching the switch 512 to initial control mode 510 and modifying the process again).

Regarding claims 17-22, these claims for "an apparatus comprising: circuitry that generates a first signal indicative of an initial frequency of an oscillator for an input parameter; circuitry that generates a second signal indicative of a reference frequency, wherein the circuitry that generates the first and second signals scales the initial frequency of the oscillator and scales the reference frequency at approximately the same time so that the generated signals are substantially in phase; and circuitry that adjusts the initial frequency of the oscillator based on a comparison of the first and second signals" are disclosed by Welland (Welland, apparatus as shown in Figure 1 including circuitry as in Figures 2, 4, 5, 7, 8, and with same method as disclosed in claims 1-8 above).

As for claims 34-41, these claims for "a method comprising: selecting a calibration input parameter for an oscillator based on temperature; and calibrating the oscillator based on a frequency of the oscillator at the calibration input parameter" and "an apparatus comprising: an

oscillator including configurable circuitry that defines an initial frequency of the oscillator at a calibration parameter; and temperature compensation circuitry that generates the calibration parameter based on temperature" are rejected for the reasons given in the scope of claims 1-8 in view of Welland and Binder as disclosed in details above.

4. Claims 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Welland (US Patent 6,137,372) in view of Binder (US Patent 5,892,408) and Fridi (US Patent 6,545,547 B2).

As for claims 42-45, Welland does not further show these features of enabling a phase locked loop following the calibration of the oscillator and/or selecting the high and low calibration voltage as noted; however, Fridi teaches these technique (Figs. 2-3 and col. 1/lines 15-40 and col. 2/line 20 to col. 3/line 41). Therefore, it would have been obvious to one of ordinary skill in the art to modify Welland's system with Fridi's teaching technique in order to enabling a phase locked loop following the calibration of the oscillator and/or selecting the high and low calibration voltage.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Norman, Sridharan et al, Keskula et al., Muyshondt et al., and Ma et al. (PTO-892) disclose VCO, temperature effects and techniques.

6. **Any response to this action should be mailed to:**
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to the New Central Fax number:

(571) 273-8300, (for Technology Center 2600 only)

Hand deliveries must be made to Customer Service Window,
Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony Thuan Nguyen whose telephone number is (571) 272-7895. The examiner can normally be reached on Monday-Friday from 9:30 AM to 7:00 PM, with alternate Fridays off.

The Art Unit location of your application in the USPTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Division or Art Unit 2618.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TONY T. NGUYEN
PATENT EXAMINER

Tony T. Nguyen
Art Unit 2618
October 23, 2006